Amendments to the Claims

Claims 1-2 (*Cancelled*)

3. (*Previously Presented*) A method of manufacturing a cellular trench-gate transistor comprising a silicon semiconductor body having an array of transistor cells (TC), the cells being bounded by a pattern of array trenches lined with insulating material within the array, the array trenches extending from an upper surface of the semiconductor body through a channel accommodating body region into an underlying drain drift region, the insulating material in each array trench providing a thin gate dielectric insulating layer on a trench sidewall adjacent the channel accommodating body region and a thick insulating layer on a trench sidewall adjacent the drain drift region, conductive material in each array trench providing a gate electrode on the thin trench sidewall insulating layer and a field plate on the thick trench sidewall insulating layer, wherein the method includes the steps of:

(a) providing a hardmask on the upper surface of the semiconductor body, then forming the array trenches by etching using the hardmask, and then. removing the hardmask;

(b) providing an integral first layer of silicon dioxide which extends on the upper surface of the semiconductor body, over the top corners of the array trenches, and over the sidewalls and the base of each of the array trenches, the first layer of silicon dioxide providing the thin gate dielectric insulating layer in the manufactured transistor;

(c) providing a layer of silicon nitride over the first layer of silicon dioxide and then providing a second layer of silicon dioxide over the silicon nitride layer;

(d) providing conductive material in each array trench to form the thin field plate ;

(e) selectively etching the second silicon dioxide layer and then the silicon nitride layer above the thin field plates such that the thick trench sidewall insulating layer has a stack of the first silicon dioxide layer, the silicon nitride layer and the second silicon dioxide layer; and then

(f) providing conductive material in each array trench to form the thick gate electrode.

4. (*Previously Presented*) The method as recited in claim 3, wherein the hardmask used in step (a) is a single silicon dioxide layer.

5. (*Previously Presented*) The method as recited in claim 3, including the further step of:

(g) forming layers for the channel accommodating body region and source regions for the transistor cells through the first layer of silicon dioxide on the upper surface of the semiconductor body.

6. (*Previously Presented*) The method as recited in claim 3, wherein steps for forming an edge termination for the transistor include:

(h) forming a perimeter trench around the array of transistor cells (TC) during step (a) and using the same hardmask;

(i) providing the first layer of silicon dioxide, the layer of silicon nitride and second layer of silicon dioxide around a top corner of the perimeter trench and on to the upper surface at the edge of the semiconductor body during steps (b) and (c);

(j) providing conductive material in the perimeter trench by means of step (d);

(k) allowing the stack of the first silicon dioxide layer, the silicon nitride layer and the second silicon dioxide layer to remain around a top corner of the perimeter trench and on the upper surface at the edge of the semiconductor body during the selective etching of step (e); and

(I) providing conductive material on the stack around the top corner of the perimeter trench to provide an edge field plate for the transistor at the same time as forming the thick gate electrode in the array trenches during step (f).

Claims 7-9 (*Cancelled*)